IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A data processing apparatus comprising:

an operation processing unit ~~having at least~~ connected to a data bus and configured to perform a read cycle ~~period when~~ by outputting a read control signal to a memory to read a read data word output by said memory to said data bus ~~said operation processing unit reads data from a device~~, and a write cycle ~~period when said operation processing unit writes~~ by outputting a write control signal to said memory and a write data word to said data bus to write said write data word in the ~~device~~ memory;

~~a memory which performs data transmission/ reception between said operation processing unit and said memory;~~

~~a data bus connected to said operation processing unit and said memory;~~ and

a pseudo-data generating circuit connected to said data bus, said read control signal output from said operation processing unit, and said write control signal output from said operation processing unit, said pseudo-data generating circuit ~~which generates~~ configured to generate pseudo-data and ~~outputs~~ output the generated pseudo-data to said data bus ~~in a time interval~~ according to an output timing based on said read control signal and said write control signal output from said operation processing unit, the output timing controlled to occur between ~~the~~ a read cycle ~~period~~ and ~~the~~ an immediately following write cycle ~~period~~, between ~~the~~ a write cycle ~~period~~ and ~~the~~ an immediately following read cycle ~~period~~, between ~~two~~ a read cycle ~~periods~~ and an immediately following read cycle, or between ~~two~~ a write cycle ~~periods~~ and an immediately following write cycle.

Claim 2 (Original): The data processing apparatus according to claim 1, wherein said pseudo-data generating circuit generates random number data as the pseudo-data.

Claim 3 (Currently Amended): A data processing apparatus comprising:

an operation processing unit ~~which performs~~ configured to perform an operation processing and output a read signal and a write signal;

~~a memory which performs data transmission/ reception between said operation processing unit and said memory;~~

a data bus connected to said operation processing unit ~~and said memory~~;

~~a read signal line and a write signal line connected to said operation processing unit and said memory;~~

a memory configured to receive the read signal and the write signal from the operation processing unit and configured to output a read data on the data bus in response to the read signal, and store a write data from the data bus in response to the write signal;

a control signal generating circuit ~~connected~~ configured to receive said read signal ~~line~~ and said write signal ~~line~~ from the operation processing unit, ~~said control signal generating circuit detects~~ detect a change in ~~a~~ the read ~~control~~ signal or a change in the write signal, and ~~a write control signal transmitted to said read signal line and said write signal line, respectively, and then generates~~ generate a control signal based on the detected change; and

a pseudo-data generating circuit connected to said ~~control signal generating circuit so as~~ data bus and configured to receive the control signal ~~and connected to said data bus~~ from the control signal generating circuit, ~~said pseudo-data generating circuit generates~~ generate pseudo-data, and ~~outputs~~ output the generated pseudo-data to said data bus in accordance with the control signal.

Claim 4 (Original): The data processing apparatus according to claim 3, wherein said pseudo-data generating circuit generates random number data as the pseudo-data.

Claims 5-10 (Canceled).

Claim 11 (Currently Amended): A memory card comprising:

an operation processing unit ~~having at least~~ connected to a data bus and configured to perform a read cycle ~~period when~~ by outputting a read control signal to a memory to read a read data word output by said memory to said data bus ~~said operation processing unit reads data from a device~~, and a write cycle ~~period when said operation processing unit writes~~ by outputting a write control signal to said memory and a write data word to said data bus to write said write data word in the ~~device~~ memory;

~~a memory which performs data transmission/reception between said operation processing unit and said memory;~~

~~a data bus connected to said operation processing unit and said memory;~~

an input/output circuit connected to said data bus, said input/output circuit ~~outputs~~ configured to input external data onto said data bus and ~~outputs~~ output data on said data bus to an external apparatus; and

a pseudo-data generating circuit connected to said data bus, said read control signal output from said operation processing unit, and said write control signal output from said operation processing unit, said pseudo-data generating circuit ~~generates~~ configured to generate pseudo-data and ~~outputs~~ output the generated pseudo-data to said data bus ~~in a time interval~~ according to an output timing based on said read control signal and said write control

signal output from said operation processing unit, the output timing controlled to occur between ~~the~~ a read cycle ~~period~~ and ~~the~~ an immediately following write cycle ~~period~~, between ~~the~~ a write cycle ~~period~~ and ~~the~~ an immediately following read cycle ~~period~~, between ~~two~~ a read cycle ~~periods~~ and an immediately following read cycle, or between ~~two~~ a write cycle ~~periods~~ and an immediately following write cycle.

Claim 12 (Original): The memory card according to claim 11, wherein said pseudo-data generating circuit generates random number data as the pseudo-data.

Claim 13 (Currently Amended): A memory card comprising:

an operation processing unit ~~which performs~~ configured to perform an operation processing and output a read signal and a write signal;

~~a memory which performs data transmission/ reception between said operation processing unit and said memory;~~

a data bus connected to said operation processing unit ~~and said memory~~;

an input/output circuit connected to said data bus, said input/output circuit ~~outputs~~ configured to input external data onto said data bus and ~~outputs~~ output data on said data bus to an external apparatus;

~~a read signal line and a write signal line connected to said operation processing unit and said memory;~~

a memory configured to receive the read signal and the write signal from the operation processing unit and configured to output a read data on the data bus in response to the read signal, and store a write data from the data bus in response to the write signal;

a control signal generating circuit ~~connected~~ configured to receive said read signal ~~line~~ and said write signal ~~line~~ from the operation processing unit, ~~said control signal generating circuit detects~~ detect a change in ~~a~~ the read ~~control~~ signal or a change in the write signal, and ~~a write control signal transmitted to said read signal line and said write signal line, respectively, and then generates~~ generate a control signal based on the detected change; and

a pseudo-data generating circuit connected to said ~~control signal generating circuit so as~~ data bus and configured to receive the control signal ~~and connected to said data bus~~ from the control signal generating circuit, ~~said pseudo-data generating circuit generates~~ generate pseudo-data, and ~~outputs~~ output the generated pseudo-data to said data bus in accordance with the control signal.

Claim 14 (Original): The memory card according to claim 13, wherein said pseudo-data generating circuit generates random number data as the pseudo-data.

Claim 15 (New): The apparatus of claim 1, wherein:

the operation processing unit is further configured to output the read control signal to have an active read control time period and an inactive read control time period, and output the write control signal to have an active write control time period and an inactive write control time period, and

the pseudo-data generating circuit is further configured to control the output timing of the generated pseudo-data to prevent the output of the generated pseudo-data to the data bus during at least one of the active read control time period and the active write control time period.

Claim 16 (New): The apparatus of claim 15, wherein:

the pseudo-data generating circuit is further configured to control the output timing of the generated pseudo-data to be delayed by a predetermined time from at least one of the active read control time period and the active write control time period.

Claim 17 (New): The apparatus of claim 3, wherein:

the operation processing unit is further configured to output the read signal to have an active read signal time period and an inactive read signal time period, and output the write signal to have an active write signal time period and an inactive write signal time period, and

the control signal generating circuit is further configured to control an output timing of the control signal to prevent the output of the generated pseudo-data to the data bus during at least one of the active read signal time period and the active write signal time period.

Claim 18 (New): The apparatus of claim 17, wherein:

the control signal generating circuit is further configured to control the output timing of the control signal to delay the output of the generated pseudo-data by a predetermined time from at least one of the active read signal time period and the active write signal time period.

Claim 19 (New): The memory card of claim 11, wherein:

the operation processing unit is further configured to output the read control signal to have an active read control time period and an inactive read control time period, and output the write control signal to have an active write control time period and an inactive write control time period, and

the pseudo-data generating circuit is further configured to control the output timing of the generated pseudo-data to prevent the output of the generated pseudo-data to the data bus during at least one of the active read control time period and the active write control time period.

Claim 20 (New): The memory card of claim 19, wherein:

the pseudo-data generating circuit is further configured to control the output timing of the generated pseudo-data to be delayed by a predetermined time from at least one of the active read control time period and the active write control time period.

Claim 21 (New): The memory card of claim 13, wherein:

the operation processing unit is further configured to output the read signal to have an active read signal time period and an inactive read signal time period, and output the write signal to have an active write signal time period and an inactive write signal time period, and

the control signal generating circuit is further configured to control an output timing of the control signal to prevent the output of the generated pseudo-data to the data bus during at least one of the active read signal time period and the active write signal time period.

Claim 22 (New): The memory card of claim 21, wherein:

the control signal generating circuit is further configured to control the output timing of the control signal to delay the output of the generated pseudo-data by a predetermined time from at least one of the active read signal time period and the active write signal time period.